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User Manual, PCIe x16 GEN 2 Cable Adapter (HIB25x16-H/T)

OSS-PCIe-HIB25-x16-H (Host)
OSS-PCIe-HIB25-x16-T (Target)

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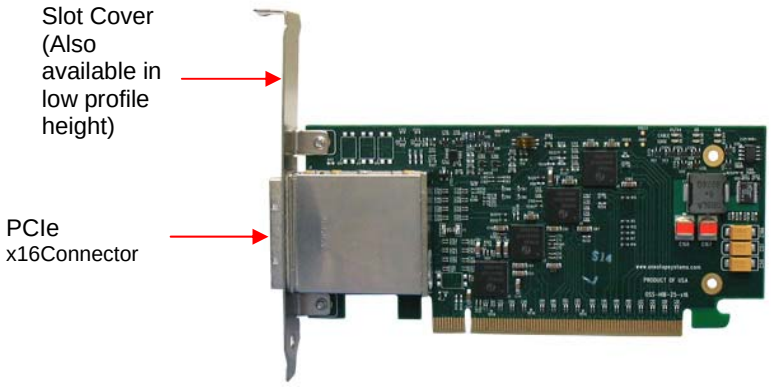
1. Overview

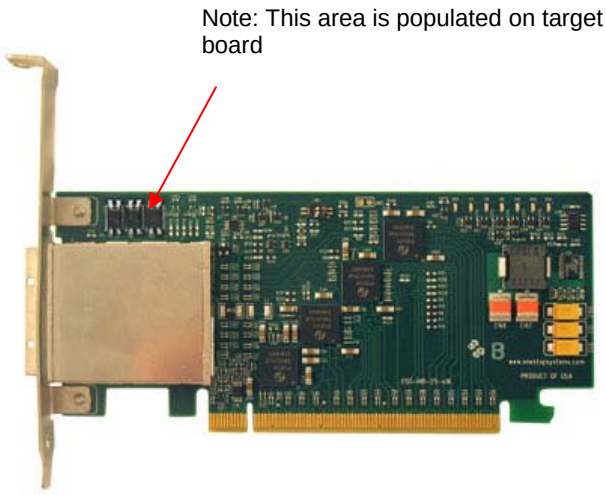
2.a. Host cable adapter

The host adapter is installed into the host computer's PCIe x16 slot. The host cable adapter (Part # OSS-PCIe-HIB25-x16-H) allows communication between a processor and an I/O point.



2.b. Target cable adapter

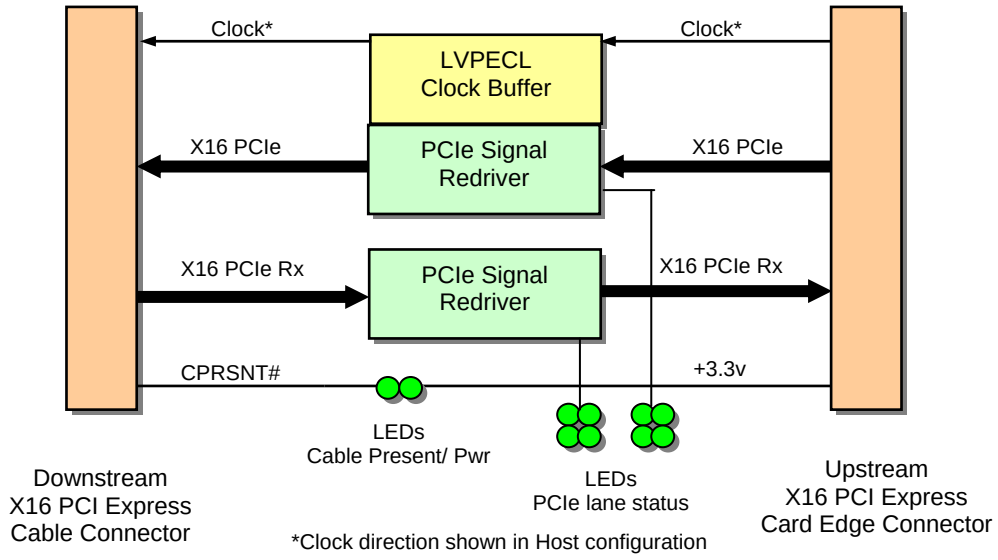
The target cable adapter (Part# OSS-PCIe-HIB25-x16-T) fits into an OSS custom 2-slot backplane and extends the PCIe bus to a single add-in board via a PCIe x16 cable.



1.a. Specifications

Dimensions (H x L): 2.2 x 4.5 inches (55 x 114mm)
Front Panel Connectors: One PCIe x16 cable connector
Front Panel Indicators: Power On / Cable Present LEDs
Power Consumption (designed to meet the following conditions) 3.75W typical, 3.3V@1.3A
Operating Environment (designed to meet the following conditions)
Temperature Range: 0° to 50°C (32° to 122°F)
Relative Humidity: 10 to 90% non-condensing
Shock: 30g acceleration peak (11ms pulse)
Vibration: 5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Redriver: Pericom PI2EQX5804
Agency Compliance: UL60950.FCC Class B, CE safety and emissions

1.b. Block Diagram



2. Initial Set-Up

2.a. Unpacking Instructions

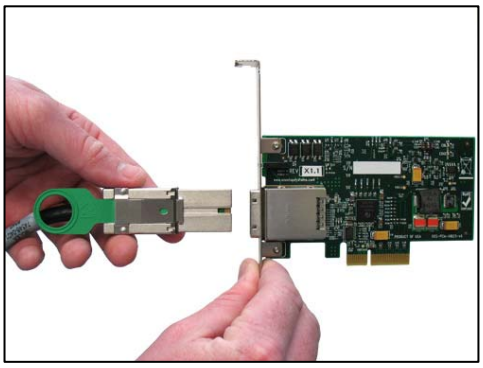
1) If the carton is damaged when you receive it, request that the carrier's agent be present when you unpack and inspect the equipment.
2) After unpacking, verify that all items listed in the packing list are present.
3) Inspect the equipment for shipping damage.
4) Save all packing material for storage or return shipment of the equipment.

Installation and Removal

1) Power down the host system.
2) Open the chassis according to your system documentation.
3) Remove the Host Cable Adapter from the protective bag, observing proper ESD safety procedures.

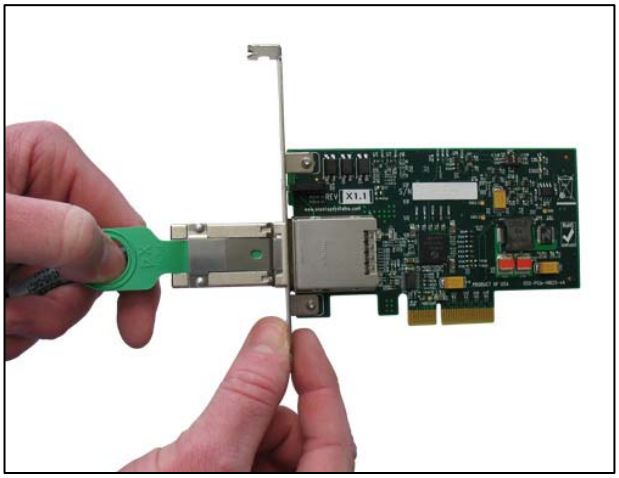
2.b. Installing the Host Cable Adapter:

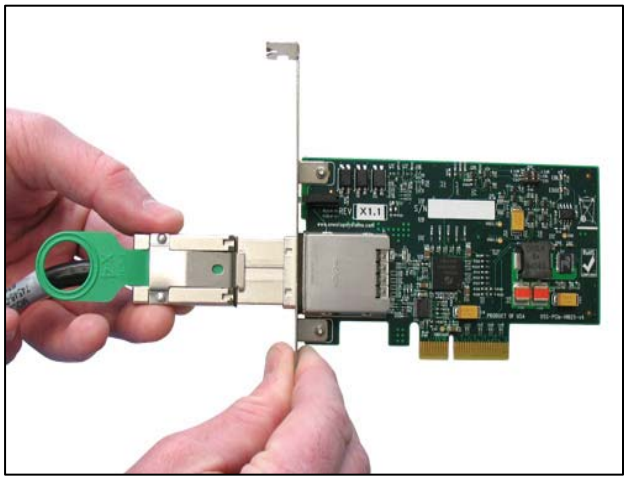
1) Insert the Host Cable Adapter into a PCIe x16 add-in card slot. Make sure that the card is well seated and tighten the screw.
2) Attach the cable by first pulling back on the retractor ring. With the keyed slot aligned with the connector key ridge on the slot cover, insert the cable connector into the cable shell on the board **until the connector teeth snap securely into the holes in the cable shell.**
3) The connectors on either end of the PCIe x16 cable are identical. Each connector is equipped with a retractor to allow the connector to be locked into place.



2.c. Removing the Host Cable Adapter

1) To remove cable pull back on green thumb tab to release metal pins and gently separate.





2) Loosen and remove the screw before removing the Host Cable Adapter from the card slot.

2.d. When using with any third party I/O device:

1) Install the downstream board into the appropriate PCIe slot.
2) Connect the external power source (separate from the host system power supply) to the downstream device if necessary.
3) Connect the PCIe cable to both the upstream host adapter and the downstream device.

3. Signal Adjustment

3.a. Signal Adjustment

The following chart indicates the default settings for the signal equalization.

SEL_2[A:D]	SEL_1[A:D]	SEL_0[A:D]	@1.25GHZ	@2.5GHZ	
0	0	0	0.5dB	1.2dB	Edge Default
0	0	1	0.6dB	1.5dB	
0	1	0	1.0dB	2.6dB	
0	1	1	1.9dB	4.3dB	
1	0	0	2.8dB	5.8dB	
1	0	1	3.6dB	7.1dB	Cable Default
1	1	0	5.0dB	9.0dB	
1	1	1	7.7dB	12.3dB	

Table 1: Equalizer Selection (refer to call-out on photo)

The following chart indicates the default settings of the 2-position dip switches for output swing control.

S_1[A:D]	S_0[A:D]	Swing (Diff. VPP)	
0	0	1V	Cable Default
0	1	05V	
1	0	0.7V	Edge Default
1	1	0.9V	

Table 2: Output Swing Control (refer to call-out on photo)

The following chart indicates the default setting for de-emphasis adjustment

D2_[A:D]	D1_[A:D]	D0_[A;D]	De-emphasis	
0	0	0	0dB	SW=ON Default
0	0	1	-2.5dB	
0	1	0	-3.5dB	
0	1	1	-4.5dB	
1	0	0	-5.5dB	
1	0	1	-6.5dB	SW=OFF Default
1	1	0	-7.5dB	
1	1	1	-8.5dB	

Table 3: De-emphasis Adjustment (refer to call-out on photo)

4. Ordering Information

OSS - PCIe-HIB25-x16 - H - One Stop Systems HIB25x16 host cable adapter.

OSS - PCIe-HIB25-x16 - T - One Stop Systems HIB25x16 host cable adapter.

Appendix

4.c. Pin Assignments

Connectors PCIe x16 Card Edge Connector

- The pins are numbered as shown with side A on the top of the centerline on the solder side of the board and side B on the bottom of the centerline on the component side of the board.
- The PCIe interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention: “PE” stands for PCIe high speed, “T” for Transmitter, “R” for Receiver, “p” for positive (+), and “n” for negative (-).
- Note that adjacent differential pairs are separated by two ground pins to manage the connector crosstalk.

Table 1: Pin-out for the PCIe x16 Card Edge Connector on the Host Cable Adapter

Pin #	Side B		Side A	
	Name	**Description**	**Name**	**Description**
1	N/C	N/C	PRSNT1#	Hot-Plug presence detect
2	N/C	N/C	N/C	N/C
3	N/C	N/C	N/C	N/C
4	GND	Ground	GND	Ground
5	NC	N/C	N/C	Not connected
6	N/C	N/C	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	3.3 V power	N/C	Not connected
9	N/C	Not connected	N/C	Not connected
10	3.3Vaux	3.3 V auxiliary power	+3.3V	3.3 V power
11	N/C	N/C	PERST#	Fundamental reset
Mechanical key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential pair, Lane 1	RSVD	Reserved
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	

27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	RSVD	Reserved	PERn3	
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved

Notes:

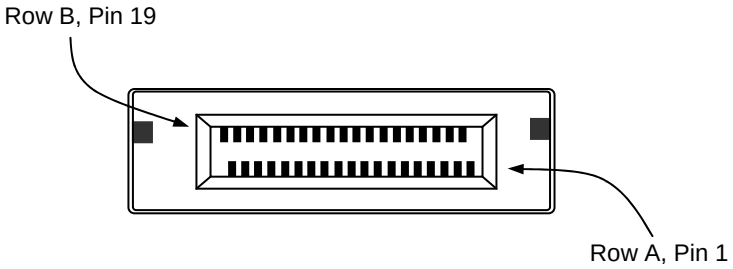
1 Optional signals that are not implemented are to be left as no connects on the board side connector.

2 Reserved signals must be left as no connects on the board side connector.

3 Although support of CWAKE# is optional from the board side connector perspective, an allocated wire is mandated for the cable assembly.

4 Board side pin-out on both sides of the Link is identical. The cable assembly incorporates a null modem for the PCIe transmit and receive pairs.

PCI Express x16 Connector Pin Assignment



PIN- out for the PCIe x16 Cable

Designator	Description	Dimension (mm)	Tolerance (mm)
C01	Interface Width	28.40	±0.10
D01	Forward Edge of Plug to Forward Lower Tab	0.75	±0.13
D02	Slot Depth	6.79	±0.13
D04	Forward Lower Tab Width	25.53	±0.13
D06	Snout Length	28.31	±0.13
D07	Snout Width	34.44	+0.20/-0.05
D08	Latch Face Plane to Forward Edge of PCB	26.29	±0.20
D09	Plug Width	53.00	±0.05
D10	Plug Thickness	20.23	±0.13
D11	Top of Plug to Bottom of Snout	17.18	±0.13
D12	Side Rail Groove Length	27.60	±0.10
D13	Snout Thickness	9.99	+0.15/-0.05
D15	Thickness Top Forward Edge of Plug	0.80	±0.05
D16	Top of Rail Groove to Top of Tongue	6.83	+0.15/-0.05

D17	D17 Top of Snout to Top of Side Groove	2.50	±0.05
D18	Top of Side Groove to Centerline of Upper PCB	0.53	±0.13
D19	Side Rail Groove Width	2.05	±0.05
D21	Zone A Internal Width Rail Groove to Rail Groove	33.24	±0.05
D21	Zone B Internal Width Rail Groove to Rail Groove	32.74	±0.05
D23	Top of Side Groove to Centerline of Lower PCB	5.03	±0.13
D27	Latch Barb Spacing	17.50	±0.05
D28	Length of Zone A	21.54	±0.13
D29	Length of Zone B	5.00	±0.13
D30	Chamfer Width	0.30	±0.05
D31	Chamfer Length	1.00	±0.05
D32	Latch to Plug Body	1.60	±0.13
D33	Internal Plug Width	30.55	±0.10
D34	Chamfer Height	0.20	±0.05
D35	Chamfer Width	0.45	Min
D36	Pull Radius	4.00	±0.10
D37	Pull Inner Diameter	16.52	Min
D38	Pull Outer Diameter	23.02	Max
D39	Pull Centerline to Radius	13.97	±0.10
D40	Pull Centerline to Radius	20.67	±0.10
D41	Pull Centerline to Latch	63.57	±3.00
D42	Pull Thickness	1.25	Min
D43	Text Height - PCIe	2.70	Ref
D44	Text Height - x16	5.60	Ref

Signal Descriptions

PETp(x)	PCI Express Transmit Positive signal of (x) pair.
PETn(x)	PCI Express Transmit Negative signal of (x) pair.
PERp(x)	PCI Express Receive Positive signal of (x) pair.
PERn(x)	PCI Express Receive Negative signal of (x) pair.
CREFCLK+/-	Cable REFerence CLocK: Provides a reference clock from the host system to the remote system.
SB_RTN	Side Band ReTurN: return path for single ended signals from remote systems.
CPRSNT#	Cable PReSeNT: Indicates the presence of a device beyond the cable.
PWR	PoWeR: Provides local power for in-cable redriver circuits. Only needed on long cables. Power does not go across the cable.)
PWR_RTN	PoWeR ReTurN: Provides local power return path for PWR pins.
CWAKE#	Cable WAKE
CPERST#	Cable PCI Express Reset